VERTICAL TRANSISTOR WITH HORIZONTAL GATE LAYERS

Abstract of the Disclosure

Vertical body transistors with adjacent horizontal gate layers are used to form a memory array in a high density flash electrically erasable and programmable read only memory (EEPROM) or a logic array in a high density field programmable logic array (FPLA). The transistor is a field-effect transistor (FET) having an electrically isolated (floating) gate that controls electrical conduction between source regions and drain regions. If a particular floating gate is charged with stored electrons, then the transistor will not turn on and will provide an indication of the stored data at this location in the memory array within the EEPROM or will act as the absence of a transistor at this location in the logic array within the FPLA. The memory array or the logic array includes densely packed cells, each cell having a semiconductor pillar providing shared source and drain regions for two vertical body transistors that have control gates overlaying floating gates distributed on opposing sides of the semiconductor pillar. Both bulk semiconductor and silicon-on-insulator embodiments are provided. If a floating gate transistor is used to store a single bit of data or to represent a logic function, an area of only $2F^2$ is needed per respective bit of data or bit of logic, where F is the minimum lithographic feature size.

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